CHAPTER 5. CIRCUIT DESCRIPTION

[1] Circuit description

1. General description

The compact design of the control PWB is obtained by using Risc Processor (CPU) in the main control section and high density printing of surface mounting parts. Each PWB is independent according to its function as shown in Fig. 1.

2. PWB configuration

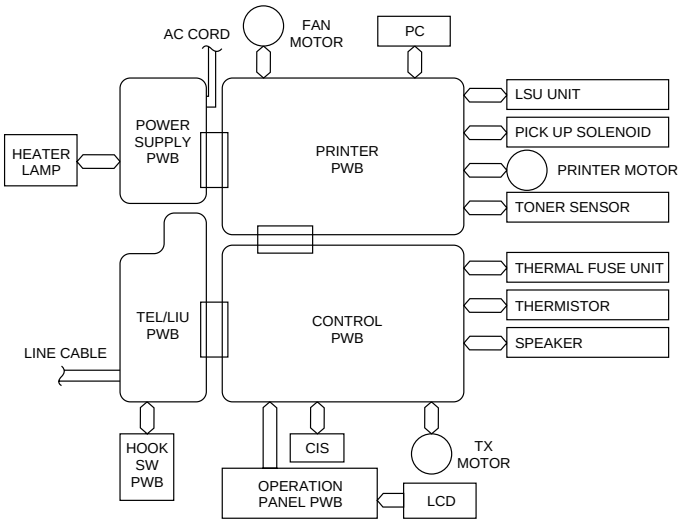


Fig. 1

(1) Control PWB

The control PWB controls peripheral PWBs, mechanical parts, transmission, and performs overall control of the unit.
This machine employs a 1-chip modem (FM214) which is installed on the control PWB.

(2) TEL/LIU and Hook SW PWB

This PWB controls connection of the telephone line to the unit.

(3) Power supply PWB

This PWB provides voltages of +5V, VREG and +24V to the another PWB.

(4) Panel PWB

The panel PWB allows input of the operation keys.

(5) Printer PWB

This PWB controls the printer mechanical parts.
This PWB employs 8 bit CPU that is installed on printer PWB.
This CPU control a printer mechanical parts.

(6) LCD PWB

This PWB controls the LCD display.

3. Operational description

Operational descriptions are given below:

- Transmission operation

  When a document is loaded in standby mode, the state of the document sensor is sensed via the ASIC (IC15).
  If the sensor signal was on, the motor is started to bring the document into the standby position. With depression of the START key in the off-hook state, transmission takes place.

  Then, the procedure is sent out from the modem and the motor is rotated to move the document down to the scan line. In the scan processor, the signal scanned by the CIS is sent to the internal image processor and the AD converter to convert the analog signal into binary data. This binary data is transferred from the scan processor to the image buffer within the RAM and encoded and stored in the transmit buffer of the RAM. The data is then converted from parallel to serial form by the modem where the serial data is modulated and sent onto the line.

- Receive operation

  There are two ways of starting reception, manual and automatic.
  Depression of the START key in the off-hook mode in the case of manual receive mode, or CI signal detection by the LIU in the automatic receive mode.

  First, the CPU(SH2) controls the procedure signals from the modem to be ready to receive data. When the program goes into phase C, the serial data from the modem is converted to parallel form in the modem interface of the 1 fax CPU(SH2) which is stored in the receive buffer of the RAM. The data in the receive buffer is decoded software-wise to reproduce it as binary image data in the image buffer. The data is DMA transferred to the recording processor within the ASIC (IC15) and sent to the LSU on printer PWB.
  CPU (SH2) and ASIC (IC15) control printing data, LSU, main motor, high-voltage circuit, heater control and fan motor.

- Copy operation

  To make a copy on this facsimile, the COPY key is pressed when the machine is in stand-by with a document on the document table and the telephone set is in the on-hook state.

  First, depression of the COPY key advances the document to the scan line. Similar to the transmitting operation, the image signal from the CIS is converted to a binary signal in the DMA mode via the reading processor which is then sent to the image buffer of the RAM. Next, the data is transferred to the ASIC in the DMA mode to send the image data to the printer PWB in order to print. The copying takes place as the operation is repeated.

[2] Circuit description of control PWB

1. General description

Fig. 2 shows the functional blocks of the control PWB, which is composed of 5 blocks.

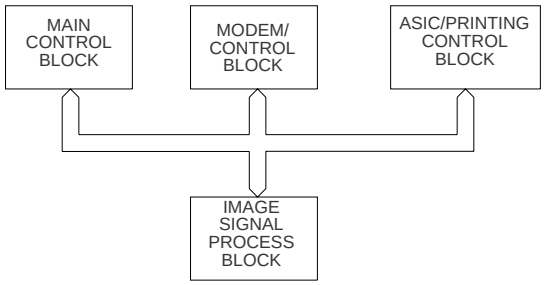


Fig. 2 Control PWB functional block diagram

2. Description of each block

(1) Main control block

The main control block is composed of HITACHI CPU (SH2), ROMX1 (8M bit), SRAMX1 (1M bit), DRAMX2 (4M bit). Devices are connected to the bus to control the whole unit.

1) SH7041 (IC5) : pin-144 QFP

The CPU Integrated Facsimile Controllers.

SH7041, contains an internal 32 bit microprocessor with an external 16 bit address space and dedicated circuitry optimized for facsimile image processing and facsimile machine control and monitoring.

2) M27C800-90F1 (IC14): pin-42 DIP (ROM)

EPROM of 8M bit equipped with software for the main CPU.

3) W24010S-70LET (IC1): pin-32 SOP (RAM)

Line memory for the main CPU system RAM area and coding/decoding process. Used as the transmission buffer.

Memory of recorded data such as daily report and auto dials. When the power is turned off, this memory is backed up by the lithium battery.

4) MSM5118165D (IC11, IC13, and system control): pin-42 SOJ (RAM)

Image memory for recording process.

- Memory for recording pixel data at without paper.

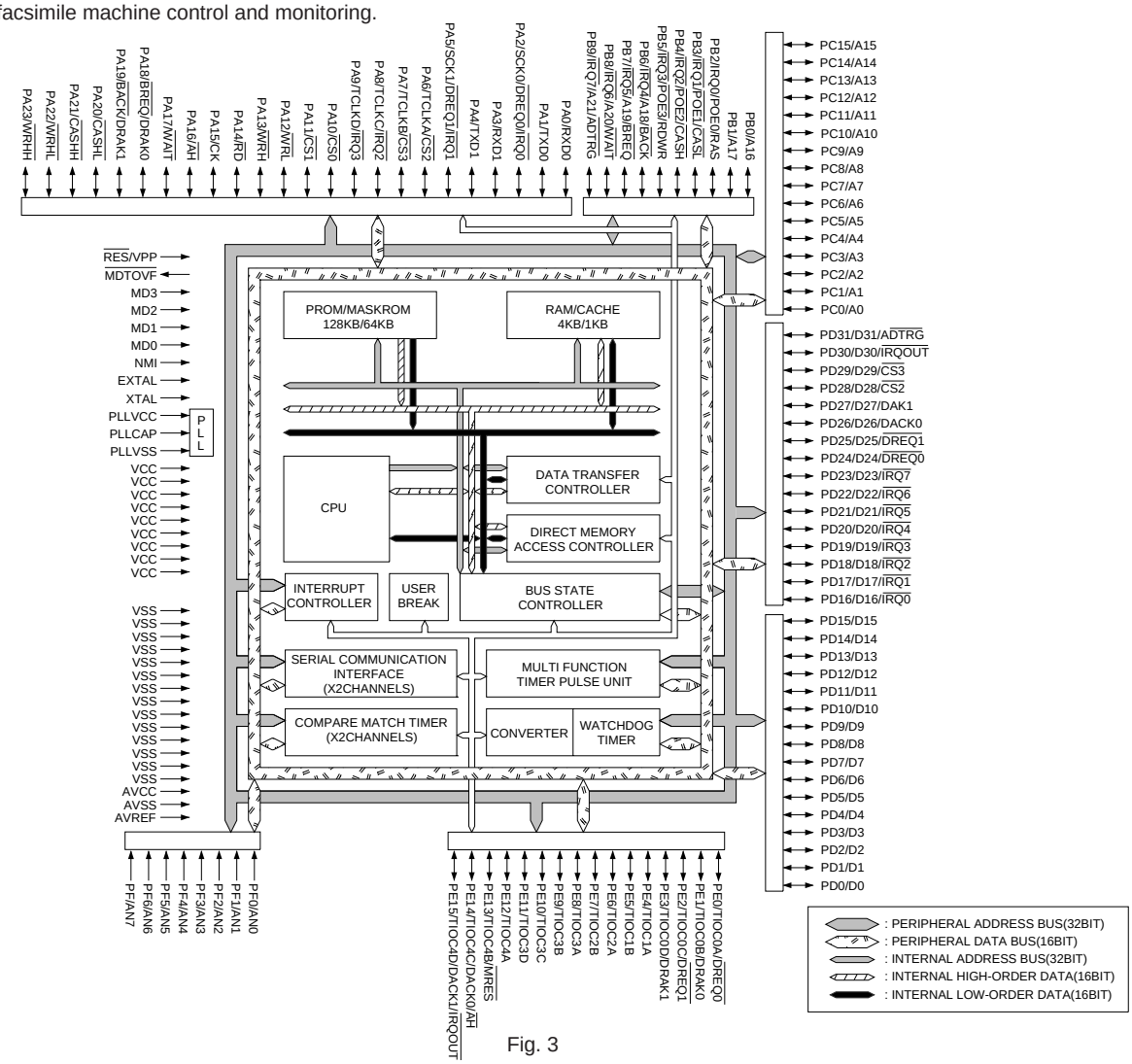


Fig. 3

SH7041 (IC5) Terminal descriptions

Classification	Code	Terminal No.	I/O	Name	Function
Power	Vcc	12,26,40, 63,77,85, 99,112,135	I	Power	Connect Vcc terminals with the power source for all systems. If any open terminal remained, operation is impossible.
	Vss	6,14,28, 35,42,55, 61,71,79, 87,93,117, 129,141	I	Ground	Connect to the ground. Connect Vss terminals with the ground for all systems. If any open terminal remained, operation is impossible.
	Vpp		I	Program power source	Connected with the power source (Vcc) for normal operation. In case of PROM mode, apply 12.5 V.
Clock	PLL Vcc	104	I	PLL power	Power source for the built-in PLL oscillator.
	PLL Vss	106	I	PLL ground	Ground for the built-in PLL oscillator.
	PLLCAP	105	I	PLL capacity	External capacity terminal for the built-in PLL oscillator.
	EXTAL	96	I	External clock	Connected with the crystal oscillator. By EXTAL terminal the external clock can be input.
	XTAL	94	I	Crystal	Connected with the crystal oscillator.
	CK	107	O	System clock	Supplied to peripheral devices.
System control	$\overline{\text{RES}}$	108	I	Power-on-reset	When impressing low level onto this terminal, power-on-reset condition is attained.
	$\overline{\text{MRES}}$	144	I	Manual reset	When applying low level to this terminal, manual reset condition is obtained.
	$\overline{\text{WDTOVF}}$	44	O	Watch dog timer overflow	Overflow output signal from WDT.
	$\overline{\text{BREQ}}$	33,38	I	Bus right demand	Low level obtained when external device demands to release the bus right.
	$\overline{\text{BACK}}$	30,37	O	Bus right demand acknowledge	Shows that the bus right has been released to the external device. The device outputting signal BREQ can acknowledge the pass right gained by receiving signal BACK.
Operation mode control	MD0~ MD3	95,97 102,103	I	Mode setting	The terminal to determine operation modes. Do not change the input value during operation.
Interrupt	NMI	98	I	Non-maskable interrupt	Non-maskable interruption demand terminal. Receiving on either leading edge or trailing edge can be selected.
	$\overline{\text{IRQ0}}$ ~ $\overline{\text{IRQ7}}$	31,32,34 37~39 41,51,52 64~69 70,72 132,136	I	Interruption demand 0 to 7	Maskable interruption demand terminal. Level input and edge input can be selected.
	$\overline{\text{IRQOUT}}$	5,46	O	Interruption demand output	Shows that the interrupt factor has occurred. During bus release, interrupt occurred can be known.
Address bus	A0~A21	7~11,13, 15~24,25, 27,29,30, 37~39,41	O	Address bus	Outputs address.

(Continuing)

SH7041 (IC5) Terminal descriptions

Classification	Code	Terminal No.	I/O	Name	Function
Data bus	D0 ~ D15 (QFP-112) D0 ~ D31 (QFP-144)	45,46 56~60, 62,64~70 72~76,78 80~84 86,88~92	O	Data bus	Bilateral data bus for 16 bit (Pin plate QFP-112) or 32 bit (Pin plate QFP-144).
Bus control	$\overline{CS0}$~$\overline{CS3}$	49,50,53 54,56,57	O	Chip select 0 to 3	Chip select signals for external memory or device.
	$\overline{RD}$	43	O	Read-out	Shows reading-out from the external device.
	$\overline{WRH}$	47	O	Higher side writing	Shows writing in higher 8 bits (bits 15 to 8).
	$\overline{WRL}$	48	O	Lower side writing	Shows writing in lower 8 bits (bits 7 to 0).
	$\overline{WAIT}$	39,101	I	Wait	To insert wait cycle into the bus cycle when accessing external space.
	$\overline{RAS}$	31	O	Low address strobe	Timing signal for low address strobe of DRAM.
	$\overline{CASH}$	34	O	Higher column address strobe	Timing signal for column address strobe of DRAM. It is output when accessing higher eight bits of data.
	$\overline{CASL}$	32	O	Lower column address strobe	Timing signal for column address strobe of DRAM.
	RDWR	36	O	DRAM read/write	Strobe signal for DRAM writing.
	$\overline{AH}$	2,100	O	Address hold	Address hold timing signal for the device using multiplex bus of address/data.
	$\overline{WRHH}$ (QFP-144)	1	O	HH writing	Shows writing of bits 31 to 24 of external data.
	$\overline{WRHL}$ (QFP-144)	3	O	HL writing	Shows writing of bits 23 to 16 of external data.
	$\overline{CASHH}$ (QFP-144)	4	O	HH column address strobe	Timing signal for column address strobe of DRAM. It is output when accessing bits 31 to 24 of data.
	$\overline{CASHL}$ (QFP-144)	29	O	HL column address strobe	Timing signal for column address strobe of DRAM. It is output when accessing bits 23 to 16 of data.
Multi function timer pulse unit	TCLKA TCLKB TCLKC TCLKD	51~54	I	MTU timer clock input	External clock input terminal for MTU counter.
	TIOC0A TIOC0B TIOC0C TIOC0D	109~111, 113	I/O	MTU input capture/ output conveyer (Channel 0)	Channel 0 terminal for inputting Input Capture/outputting Output Conveyer/outputting PWM.
	TIOC1A TIOC1B	114,115	I/O	MTU input capture/ output conveyer (Channel 1)	Channel 1 terminal for inputting Input Capture/outputting Output Conveyer/outputting PWM.
	TIOC2A TIOC1B	116,117	I/O	MTU input capture/ output conveyer (Channel 2)	Channel 2 terminal for inputting Input Capture/outputting Output Conveyer/outputting PWM.
	TIOC3A TIOC3B TIOC3C TIOC3D	138~140,	I/O	MTU input capture/ output conveyer (Channel 3)	Channel 3 terminal for inputting Input Capture/outputting Output Conveyer/outputting PWM.
	TIOC4A TIOC4B TIOC4C TIOC4D	2,5,143,144	I/O	MTU input capture/ output conveyer (Channel 4)	Channel 4 terminal for inputting Input Capture/outputting Output Conveyer/outputting PWM.
Direct memory access control (DMAC)	$\overline{DREQ0}$, $\overline{DREQ1}$	60,62,109, 111,132,136	I	DMA transfer demand (Channels 0 and 1)	Input terminal for external DMA transfer demand.
	DRAK0, DRAK1	2,30,33,110, 113	O	DREQ demand acceptance (Channels 0 and 1)	Outputs sampling acceptance of external DMA transfer demand input.
	DACK0, DACK1	5,58,59	O	DMA transfer strobe (Channels 0 and 1)	Outputs strobe to external I/O of external DMA transfer demand.

(Continuing)

SH7041 (IC5) Terminal descriptions

Classification	Code	Terminal No.	I/O	Name	Function
Serial communication interface (SCI)	TxD0, TxD1	131, 134	O	Transmitting data (Channels 0 and 1)	Output terminal for transmitting data of SC10 to 1.
	RxD0, RxD1	130, 133	I	Receiving data (Channels 0 and 1)	Input terminal for receiving data of SC10 to 1.
	SCK0, SCK1	132, 136	I/O	Serial clock (Channels 0 and 1)	Input/output terminal for clock of SC10 to 1.
A/D converter	AVcc	128	I	Analog power source	Vcc potential is connected by analog power source.
	AVss	124	I	Analog ground	Vss potential is connected by analog power source.
	AVref (QFP-144)	127	I	Analog reference power source	Input terminal for analog reference power source.
	AN0~AN7	118~123, 125,126	I	Analog input	Analog signal input terminal.
	$\overline{\text{ADTRG}}$	41,45	I	A/D conversion trigger input	External trigger input to start A/D conversion.
I/O port	$\overline{\text{POE0}}$~ $\overline{\text{POE3}}$	31,32,34,36	I	Port output enable	Input terminal to enable general port to control driving of port terminal in case of setting output.
	PA0~PA15 (QFP-112) PA0~PA23 (QFP-144)	1,3,4,33,43, 47~54,100, 101,107, 130~134,136	I/O	General port	General input/output port terminal to specify input/output by every bit.
	PB0~PB9	25,27,31,32, 34,36~39,41	I/O	General port	General input/output port terminal to specify input/output by every bit.
	PC0~PC15	45,46,57~60,	I/O	General port	General input/output port terminal to specify input/output by every bit.
	PD0~PD15 (QFP-112) PD0~PD31 (QFP-144)	62,64~70,72, 73~76,78, 80~84,86, 88~92	I/O	Genelal port	General input/output port terminal to specify input/output by every bit.
	PE0~PE15	2,5,109~111, 113~116 137~140 142~144	I/O	General port	General input port terminal to specify input/output by every bit.
	PF0~PF7	118~123, 125,126	I	General port	General input port terminal.

(2) Panel control block

The following controls are performed by the Gate array (LR38784).

- Operation panel key scanning
- Operation panel LCD display

(3) ASIC/Printing control block

1) ASIC [LR38784 208pin (embedded gate array) functions(IC15)

① Mapper
Mapping can connect the modem and image handing LSI to a domain of CS2 (Chip Select 2).

② Real-time-clock interface
This interface has the clock-synchronous type serial transfer mode and can write and read to the CLOCK IC (SM8578BV or NJU6355).

③ Image handing LSI interface
This interface has parallel or serial transfer mode with the image handing LSI.

④ GDI ASIC
This function GDI i/f for PC printing only.

⑤ IEEE1284
This function IEEE 1284 i/f for PC scanning and PC fax.

⑥ Sending motor control
This function outputs the sending motor control signals of 2 or 1-2 phase excitation to the motor driver.

⑦ Buzzer and Ringer control
This function outputs a buzzer (1042Hz) or a ringer (controlled signal) signal.

⑧ Laser signal control
This function controls to output laser beam.

⑨ Protection circuits
LR38784 has protection circuits for a pick-up-solenoid and a heater.

LR38784 (IC15) Terminal description

Pin No.	I/O	Signal name
1	–	GND
2	–	GND
3	I	LCPD3
4	I	LCPD4
5	I	LCDREQ
6	TO	LEDDV4
7	TO	LEDDV3
8	TO	LEDDV2
9	TO	LEDDV1
10	TO	RS
11	O	LCDACKZ
12	TO	E
13	IOR	LD3
14	–	GND
15	IOR	LD2
16	IOR	LD1
17	IOR	LD0
18	IU	SEN4Z
19	IU	SEN3Z
20	IU	SEN2Z
21	IU	SEN1Z
22	IU	SEN0Z
23	I	FRSNS
24	I	ORGSNS
25	I	B4SNS
26	I	MDMINTZ
27	O	MDMRDZ
28	O	MDMWRZ
29	O	MDMCSZ
30	O	MDMRSTZ
31	–	GND
32	IS	CK16M
33	O	OE3Z
34	O	WE3Z
35	O	BZOUT
36	I	LCINT
37	O	LCRDZ
38	O	LCWRZ
39	I	SD
40	I	SDE
41	I	SDCK
42	ID	MTST
43	I	DACK0Z
44	I	DACK1Z
45	I	DRAK0

LR38784 (IC15) Terminal description

Pin No.	I/O	Signal name
46	I	DRAK1
47	O	DREQ0Z
48	O	DREQ1Z
49	–	GND
50	IS	SHCK
51	–	GND
52	–	GND
53	–	VDD
54	–	VDD
55	O	RESET2Z
56	O	USOUT
57	O2M	INT1Z
58	O	INT2Z
59	O2M	INT3Z
60	O2M	INT4Z
61	O	INT5Z
62	I	RDZ
63	I	WRHZ
64	I	WRLZ
65	I	CS2Z
66	I	CSIZ
67	IS	WDTOVFZ
68	O	RTCIO
69	O	RTCCE
70	–	GND
71	O	RTCCK
72	IOR	RTCDT
73	ID	TEST1
74	IU	CASHZ
75	IU	CASLZ
76	IU	RASZ
77	IU	RDWRZ
78	O	BREQZ
79	I	BACKZ
80	IOR	PD0
81	IOR	PD1
82	IOR	PD2
83	IOR	PD3
84	–	GND
85	OR	PA9
86	OR	PA0
87	I	LCPD0
88	I	LCPD1
89	I	LCPD2
90	OR	PA1
91	OR	PA2

Pin No.	I/O	Signal name
92	OR	PA3
93	OR	PA4
94	OR	PA5
95	–	GND
96	OR	PA6
97	OR	PA7
98	OR	PA8
99	IOR	PD4
100	IOR	PD5
101	IOR	PD6
102	IOR	PD7
103	–	VDD
104	–	VDD
105	–	GND
106	–	GND
107	OSC3M	PEPCKO
108	OSCI	PEPCKI
109	IU	EXINT1Z
110	IS	RESETZ
111	O	PCASZ
112	O	PWRZ
113	O	PRASZ
114	O	TPA
115	O	TPB
116	O	TPAZ
117	O	TPBZ
118	–	GND
119	O	OE1Z
120	O	WE1Z
121	O	OE2Z
122	O	WE2Z
123	O	CASLOZ
124	O	RASOZ
125	O	CASHOZ
126	–	GND
127	O	PWRLY
128	O	HLON
129	O	TC_BIASON
130	O	PUS
131	O	MCON
132	I	PE
133	O	PMDZ
134	O	APCSTT
135	ICS	SYNCZ
136	O	SMAP
137	–	GND

LR38784 (IC15) Terminal description

Pin No.	I/O	Signal name
138	–	VDD
139	IOR	MA
140	IOR	MB
141	I	DOPZ
142	I	PINZ
143	I	POUTZ
144	I	XBPSTB
145	IO12MR	BPBD7
146	O	VIDEO
147	–	GND
148	IO12MR	BPBD6
149	IO12MR	BPBD5
150	IO12MR	BPBD4
151	–	GND
152	IO12MR	BPBD3
153	IO12MR	BPBD2
154	IO12MR	BPBD1
155	–	GND
156	–	GND
157	–	VDD
158	–	VDD
159	IO12MR	BPBD0
160	I	XBPAF
161	O12M	XBPOACK
162	O12M	BPOBY
163	I	XBPINI
164	–	GND
165	O12M	BPOPE
166	O12M	BPOSE
167	O12M	XBPOFT
168	I	XBPSEI
169	–	GND
170	–	VDD
171	IS	PRTCLK
172	IOR	D0
173	IOR	D1
174	IOR	D2
175	IOR	D3
176	IOR	D4
177	IOR	D5
178	IOR	D6
179	IOR	D7
180	–	GND
181	IOR	D8
182	IOR	D9
183	IOR	D10
184	IOR	D11
185	IOR	D12
186	IOR	D13
187	IOR	D14
188	IOR	D15
189	–	GND
190	I	A21
191	I	A20
192	I	A13
193	I	A12
194	I	A11
195	IOR	A10
196	IOR	A9
197	IOR	A8
198	IOR	A7
199	IOR	A6
200	–	GND
201	IOR	A5
202	IOR	A4
203	IOR	A3
204	IOR	A2
205	IOR	A1
206	I	A0
207	–	VDD
208	–	VDD

2) Printing control (PCU)

The CPU and ASIC control printing.

1. Blockdaiaglam

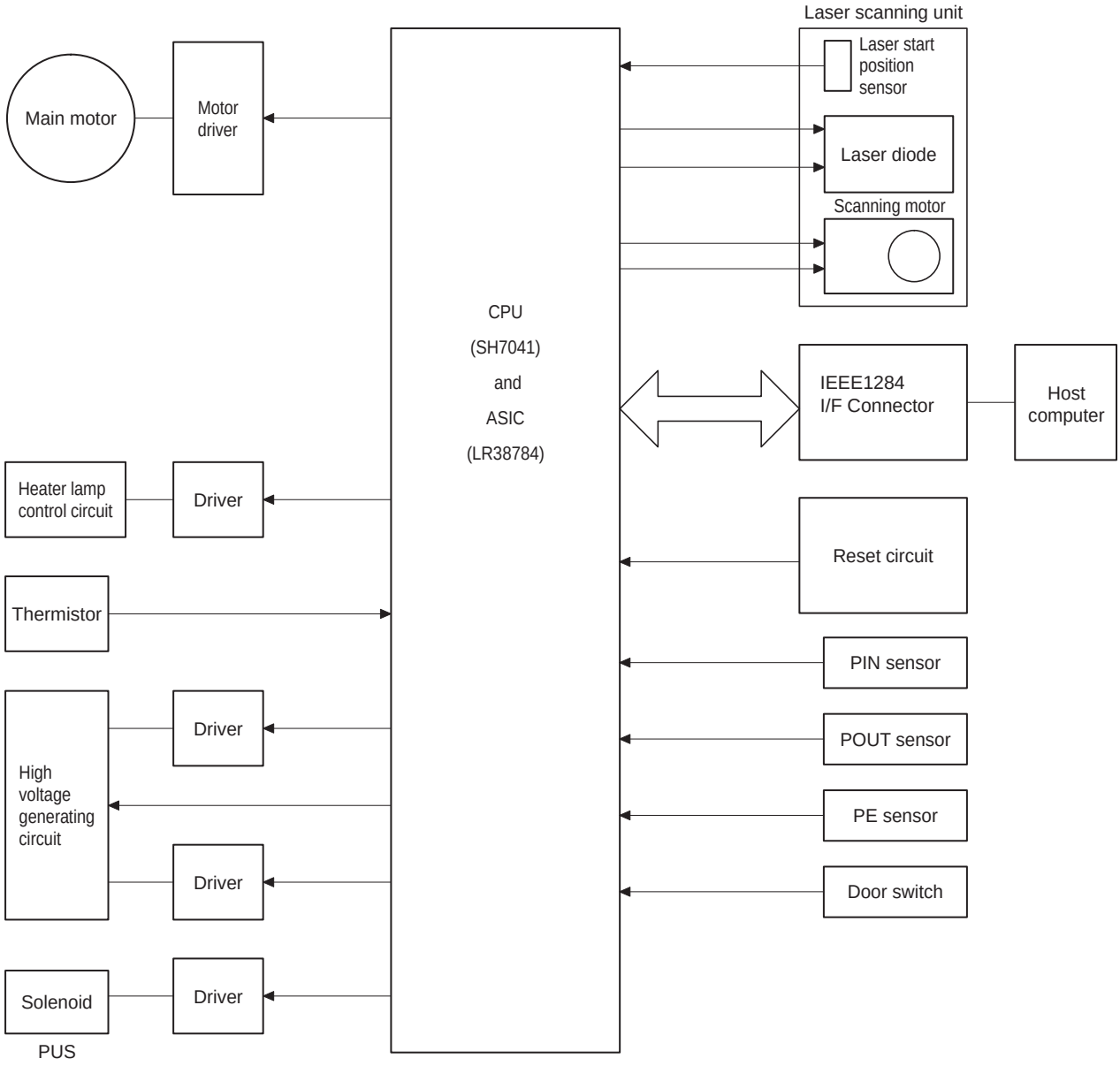


Fig. 4

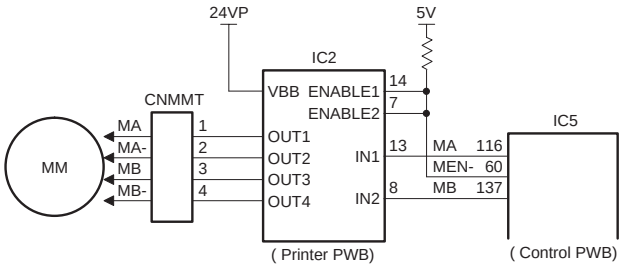
The PCU controls the following functions and items:

① Rotation of the main motor (pulse motor)
② High voltage output
③ Fusing temperature
④ Optical system (polygon motor/ laser APC circuit start)
⑤ 400/600DPI resolution automatic selection
⑥ Temperature correction of fusing temperature and high voltage output

3) Unit control

a. Main motor drive circuit

This machine uses the 4-phase pulse motor, and is driven by the following pulses and the circuit



(Drive waveform)

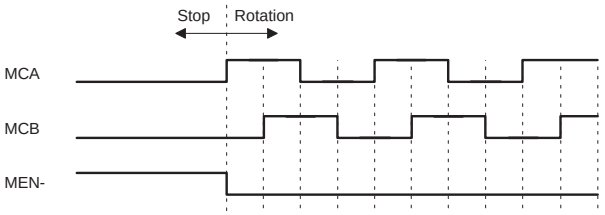


Fig. 5

b. Paper feed controller

Basically, the feed roller is rotated 1.5 times.
If interval between PUS and PIN is within 0.5 sec., it is rotated 1 time.

The procedure of clutch control
① Timer is cleared by PUS ON according to clutch control demand.
② PUS OFF 100 ms after PUS ON
③ PUS ON again 450 ms after the procedure ① above.
④ If paper is remained in PIN 500 ms after the procedure ①, the third PUS ON is stopped.
⑤ PUS OFF 1.25s after the procedure ①. Clutch control demand OFF if additional control is cancelled.
⑥ PUS ON again 1.534s after the procedure ①.
⑦ PUS OFF 2.334s after the procedure ①.
⑧ Clutch control demand OFF 3.366s after the procedure ①.

If the paper is not fed normally and the paper in detector signal (PIN_) is not outputted even with the above operation, the PCU judges it as a paper jam display is made.

The paper in detector signal (PIN_) is used for the top margin control signal in addition to jam detection.

The diagram below shows timings of clutch operation.

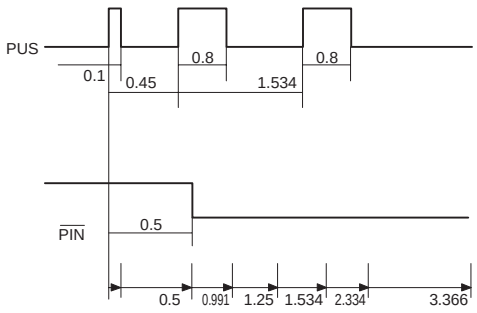


Fig. 6

c. Electrical connection

In the paper feed and transportation system, drive parts and sensors are connected as shown in the figure below.

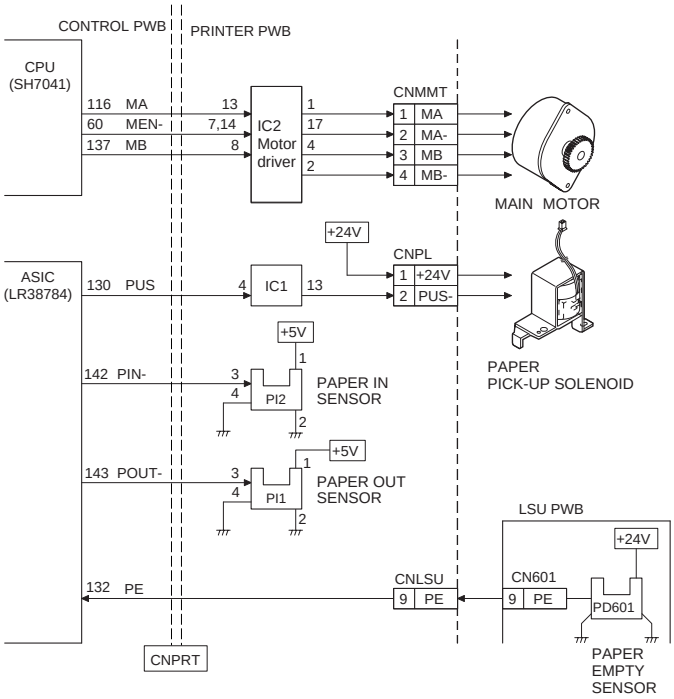


Fig. 7

- The main motor, which is the drive source for the paper feed and transportation system, is a 4-phase stepping motor in 2-phase excitement bipolar system, The step angle is 7.5°.
- The pick-up solenoid operates on 24V to turn on/off paper feed.
- There are following kinds of sensors.

Paper empty sensor (Transmission photo transistor) :

The paper empty sensor is positioned on the LSU PWB, and is used to detect presence of paper on the multi-purpose paper tray.

Paper in sensor: (Transmission photo transistor):

This sensor is used to detect the paper feed timing of the next paper (in prefeed) and to make synchronization between paper transport and image forming on the drum. This sensor is also used to detect paper jams.

Paper out sensor: (Transmission photo transistor):

This sensor senses paper exit, and paper jam.

d. High voltage unit control

The high voltage unit outputs the following voltages:

- Main charger voltage (DC-950V + AC600V peak to peak)
- Transfer charger voltage (DC+2100V + AC600V peak to peak)
- Developing bias voltage (DC-390V)

The following signals are outputted from the CPU (ASIC) to control the above voltages.

- **MCON**

  This signal is to turn on/off the main charger.

  When this signal is outputted, Q7 is driven to the high impedance state. Then Q9 conducts to drive transformer T2.

  As a result, the main charger voltage is outputted to the secondary side of the transformer.

- **TC/BIASON**

  This signal is to turn on/off the transfer charger and the developing bias voltage.

  When this signal is outputted, Q3 is driven to the high impedance state. Then Q5 is conducted to drive T1 to output the transfer charger voltage and developing bias voltage to the secondary side of the transformer.

- **PWMSIN**

  This signal is to control the main charger voltage and the transfer charger voltage. The PWM pulse of 295.28Hz is outputted.

  This pulse waveform adds the AC component to the main charger voltage and the transfer charger voltage.

  By changing the pulse duty of this signal, the main charger voltage and the transfer charger voltage are controlled (during temperature correction operation).

  When the pulse duty of this signal is changed, the collector currents of Q4 and Q8 are changed. Therefore, the base current of Q9 and the drive current of transformer T2 are changed to change the main charger voltage and the transfer charger voltage.

  R29, R31, C19, and C20 from a filter circuit which dulls the waveform of PWMSIN signal.

e. Electrical connection

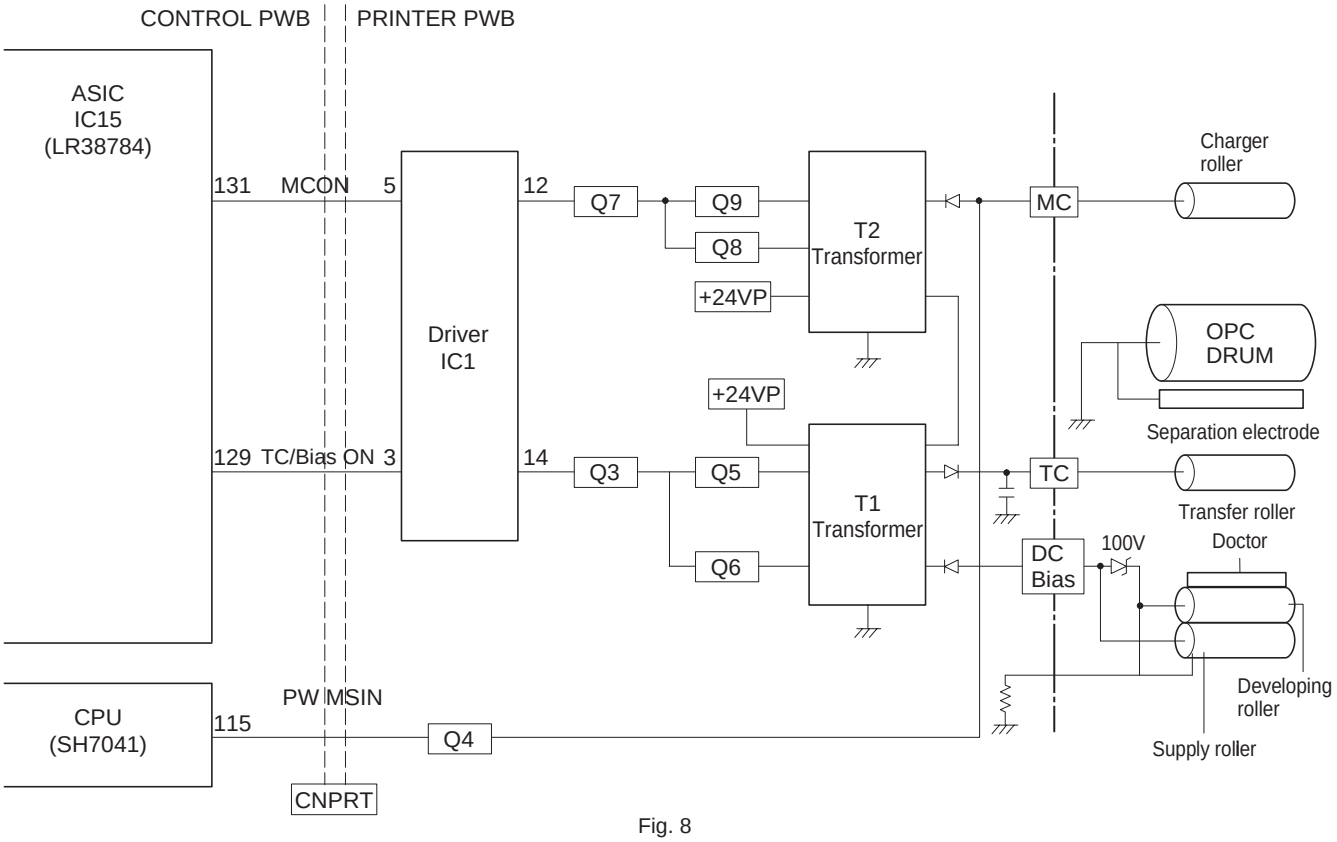


Fig. 8

f. Laser scanning unit

This unit controls the laser beam power and laser beam scanning.

The control is performed with the signals inputted outputted to or from the CPU and ASIC.

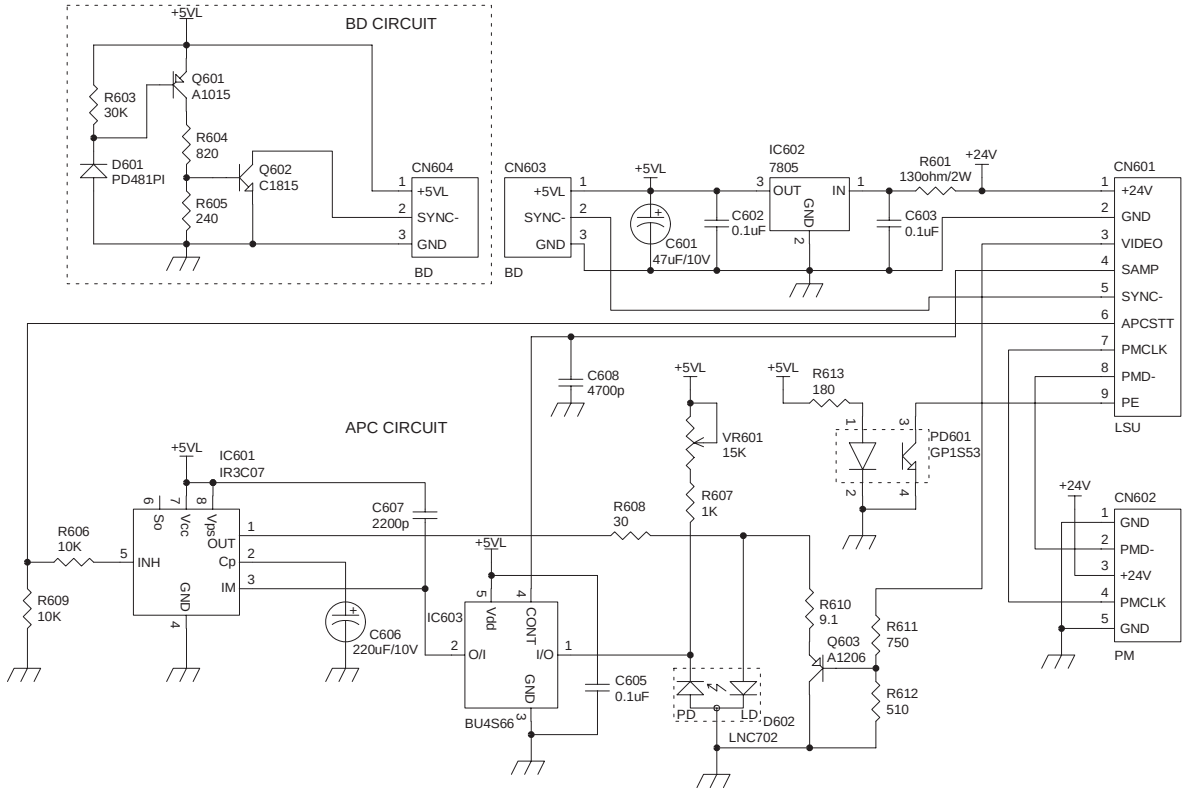


Fig. 9

1) Signal functions

PMCLK

Clock signal for driving the scanning motor. (1.77KHz)

PMD

Scanning motor ON/OFF signal.

APCSTT

Used to start the laser beam generation circuit.

SYNC

This signal is outputted when the laser beam scanned by the laser beam sensor signal is sensed by sensor (Photo diode D601).

Used for the left margin control.

VIDEO

This signal is used to control the laser diode emitting.

Not only when the laser beam is emitted to perform the LEND process, but also when the laser beam is emitted as image data, ASIC controls and the signal is outputted from video terminal.

2) Laser beam power control

The laser beam power is controlled in the laser emitting unit PWB.

This circuit functions to keep the laser beam output power at a constant level.

The laser beam output is monitored with photo diode D602 for monitor. When the laser beam output rises above the specified value, the impedance of photo diode D602 is decreased to decrease the monitor input (3PIN) voltage of the laser diode control IC (IC601).

Then the laser diode (LTO28GS) drive voltage is decreased to decrease the laser beam output to the specified level.

When the laser beam output is decreased below the specified level, the contrary operation are performed.

3) Starting operation

Warm-up operation of laser scanning is described below.

The operation is made when the cover is closed from the open state, and is made before starting printing.

The PMCLK signal is the clock signal for scanner motor speed control. It is rectangular waveform of 1.18kHz.

① The PMD_signal is to turn on/off the scanner motor. When this signal is outputted, the scanner motor is operated.

② After 2 sec of starting the scanner motor, the laser power control signal APCSTT and the laser diode ON signal VIDEO (LEND) are outputted to output laser beams.

③ After 0.5sec from outputting the VIDEO (LEND) signal and turning on the laser diode, the LEND process operation is started.

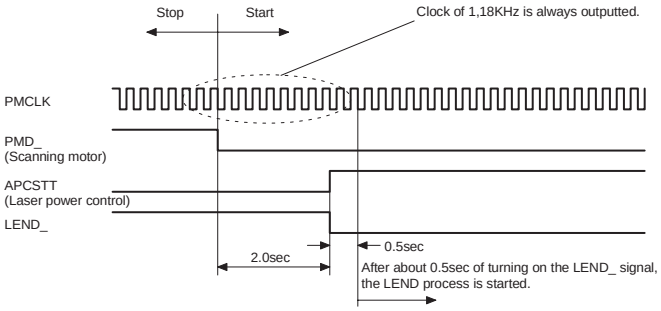


Fig. 10

4) LEND process operation

The LEND process operation means outputting the HSYNC (HSYNC_) signal for left margin control.

To control the left margin, the scanning position of the scanning mirror on the virtual area of the left side out of the margin must be precisely detected when the scanning motor reaches the stable rpm. Therefore, the dummy laser beam must be outputted to detect the position.

The laser beam scanning position is detected by the laser beam sensor, and the SYNC signal is outputted.

The dummy laser beam is outputted for every scanning of one line only when the scanning position of the scanning mirror is outside the left area of virtual paper. (The laser is forcibly turned on by the PCU when the laser beam scanned by the scanning mirror come in front of the laser beam sensor (left margin reference).)

Note: The laser beam is not outputted continuously during printing operation of one paper. It repeated ON and OFF for every scanning of one line.
The laser beam is outputted only when the LEND process for controlling the print left margin is made and when the print image is drawn on the photoconductor.

• **Laser control signal**

LEND signal is controlled based on HSYNC signal.

For simultaneous APC control, SAMP signal is also controlled.

These timings are made by ASIC. The line-end-off section is set by the register.

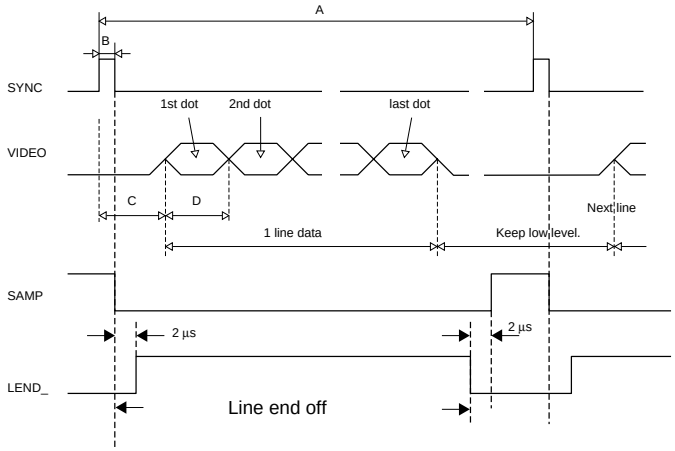


Fig. 11

① When the LEND_ signal is on, the dummy laser beam is outputted, and the scanned laser beam is detected by the laser beam sensor to output the SYNC signal. When the SYNC signal is outputted, the CPU detects the scanning position.

② At the rising of the SYNC signal, the CPU turns off the LEND_signal. By this, the dummy laser beam is turned off. When the CPU detects the scanning position with the SYNC signal, the dummy laser beam becomes unnecessary.

③ The draw signal Video_ is made from the DDATA_ signal of one line outputted from the ASIC. When it is outputted, the laser beam is turned on off accordingly. This corresponds to the making of latent electrostatic images on the photoconductor drum.

④ When making of latent electrostatic images for one line is completed, the CPU turns on the LEND_ signal before the output timing of the SYNC.

Procedures ①~④ are repeated.

Resolution	Time				
	A	B	C	D	Line end off
600dpi	846.7µs	3 ~ 10µSec	(29.97µSec)	(84.3nSec)	720µs
406.4x 391.16dpi	1298.7524µH	4.6 ~15.3µSec	(45.971µSec)	(190.907nSec)	510µs

5) Automatic acknowledgment of resolution

The CPU control 600dpi/400dpi when starting the LEND process.

When the scanner motor rotation is stabilized, the SYNC interval is judged.

g. Electrical connection

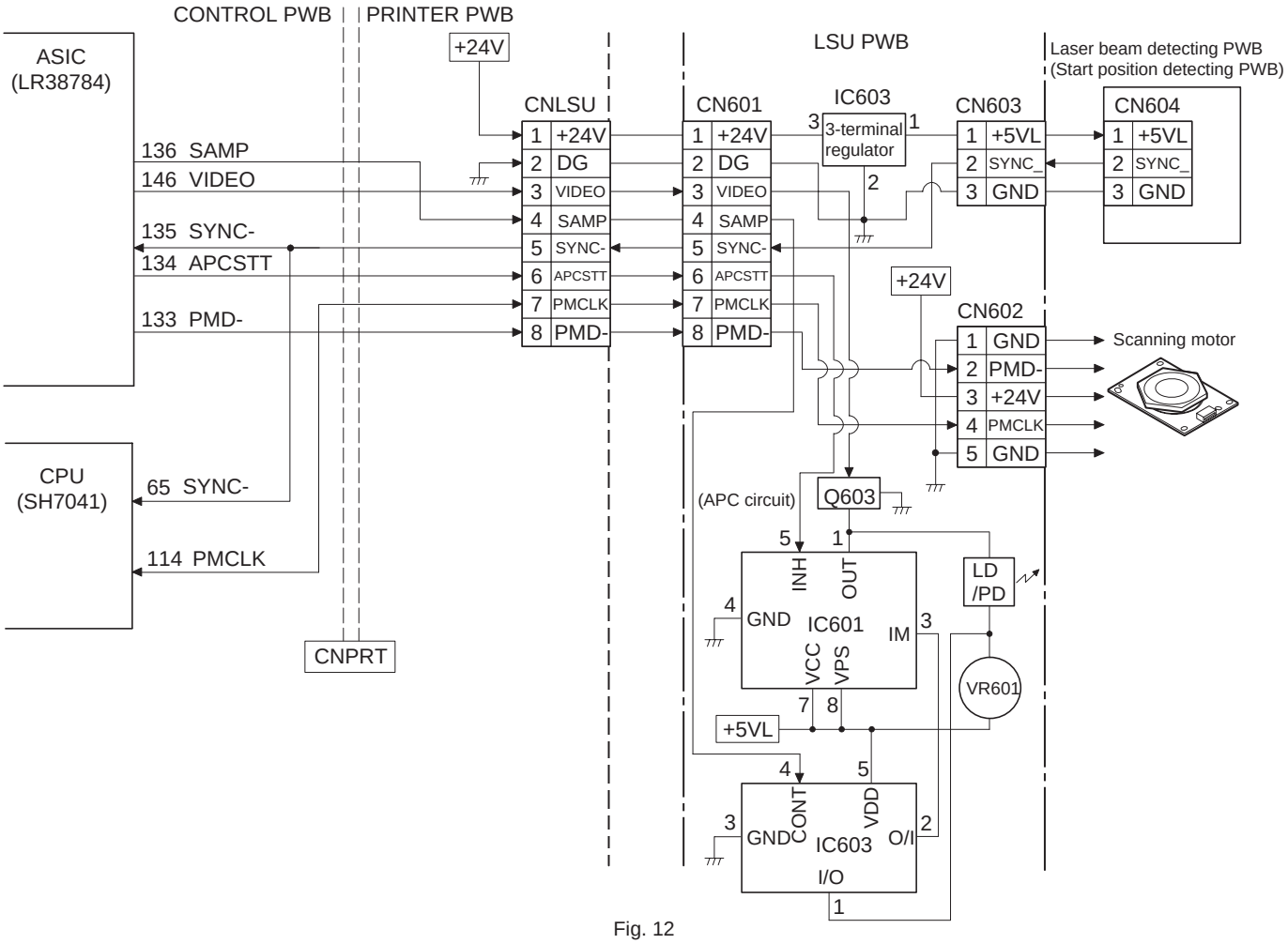


Fig. 12

The laser diode control board is driven in synchronization with the VIDEO signal sent from the CPU board.

By the operation of the laser diode control board, infrared laser beams of 780nm are outputted from the laser diode and made in parallel by the collimator lens, and focused onto the scanning motor by the first cylinder lens.

The scanning mirror rotation is controlled by the scanning motor to be constant at 11811rpm (600dpi) and 8000rpm (400dpi), and the laser beam is directed to the main scanning direction.

The scanning motor is of six-surface, and six-line print is made for one rotation of the scanning motor. The laser beam reflected by the scanning mirror is directed to the curved mirror by the first reflection mirror. Before reaching the curved mirror, the laser beam enters the photo sensor on the start position detector board, making vertical synchronization and print data synchronization (generating the SYNC signal).

The curved mirror directs the laser beam to the second reflection mirror in parallel and in even interval regardless of difference in angles of incidence from the first reflection mirror. The laser beam reflected by the second reflection mirror ia passed through the second cylinder lens to reach the photoconductor drum.

The second cylinder lens corrects blur of the images caused by variations in the installing angle due to the two-surface scanning mirror, providing stable laser beams to the photoconductor drum for each line.

h. Fusing unit control

The fusing section is heated by the heater lamp (400W). The heater lamp is controlled (turned on/off) to keep the optimum temperature. The following signals are outputted by the ASIC and CPU for control.

1) Signal functions

- **HLON**

  This signal is to turn on/off the heater lamp. When this signal is outputted, photo triac PD101 turns on to turn on triac T2. Then an AC power is supplied to the heater lamp to turn on the heater lamp.

- **RTH**

  This is the output signal of the thermistor which detects the surface temperature of the heat roller. It is inputted to the CPU. The heater lamp is turned on/off depending on the value of RTH voltage.

2) Protect against overheat

Though the heater lamp ON signal (HLON) is normal, if triac PD101 and T2 are kept ON, overheat may result.

To prevent against this, temperature fuses are used.

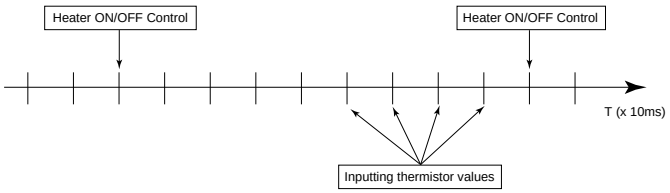
When the fusing roller surface temperature exceeds about 300 degrees C, the temperature fuse blows off to open the 12V power line which drives the power relay RY101, opening the power line for the photo triac PD101 and triac T2. Therefore, the power is not supplied to the heater lamp.

A temperature fuse is also provided in the heater lamp power line. In case of overheating, the heater lamp power line is opened directly.

3) Timing of temperature detection and heater control

As shown by the following timings, four values of software thermistor voltage are input as A/D conversion values. The mean value of two medians among these four is regarded as the newest thermistor value (temperature).

- The value is compared with the temperature (155°C) control value every 100 ms.
- If the value is higher than 155°C, the heater becomes OFF. If lower, the heater becomes ON.
- The heater ON timing is in accordance with the timing of Power Zero Cross interrupt.



Timings of thermistor value input and heater control

Fig. 13

4) Heater control (Temperature control)

Control method

① Base machine printing (Copy, List, Receiving)

- Temperature control is started when data to be printed are produced (or when slips are to be prepared).
- Temperature is controlled at 155 °C. (Heater OFF over 155 °C. Heater ON below 155 °C.)
- After printing, temperature is not controlled. (Heater is not turned ON.)
- Fan motor starts revolving from the beginning of temperature control and stops 120 seconds after printing is finished.

② PC printing

- Temperature control is started when PC starts printing.
- Temperature is controlled at 155 °C. (Heater OFF over 155 °C. Heater ON below 155 °C.
- After printing, temperature is not controlled.
- Fan motor starts revolving from the beginning of temperature control and stops 120 seconds after printing is finished.

Temperature control is not started from the start of printing because the first copying time should be within 28 seconds.

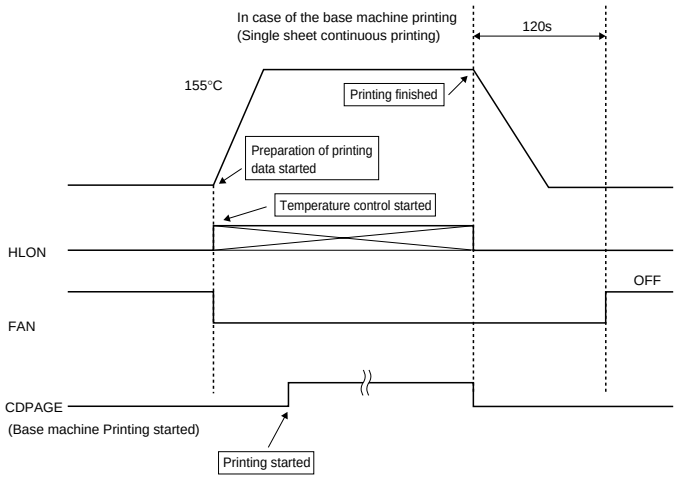
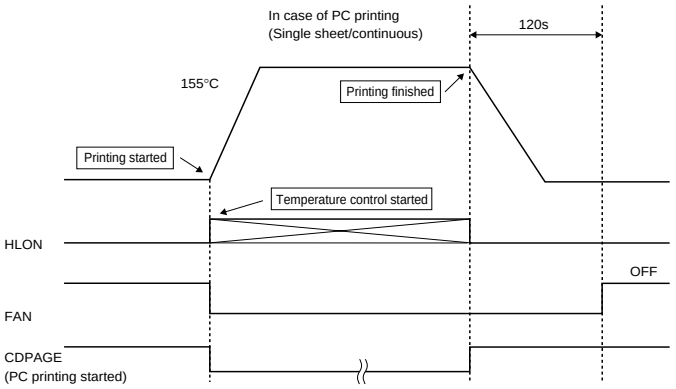


Fig. 14



The Heater ON timing is set during Zero Cross interrupt.

Fig. 15

i. Electrical connection

Heater lamp:	The 400W halogen lamp is used. This spring presses the pressure roller with a 690g pressure on one side. Teflon sheet and pressure pad: Pressure pad is covered with teflon sheet to feed paper smoothly at the time of fixing. Use of the pressure pad and the Teflon sheet enables fixing at low pressure (690 g on one side)
Thermistor:	Thermistor of chip type with good response is used to respond to rapid heating (rapid warm-up of about 8 sec) of the heat roller.
Temperature fuse 1 (132°C):	Temperature fuse 1 is installed to the fusing cover. It blows off when the ambient temperature of the fusing cover rises abnormally (132°C).
Temperature fuse 2 (187°C):	Temperature fuse 2 is in close contact with the heat roller. It blows off when the heat roller temperature rises abnormally high (187°C).

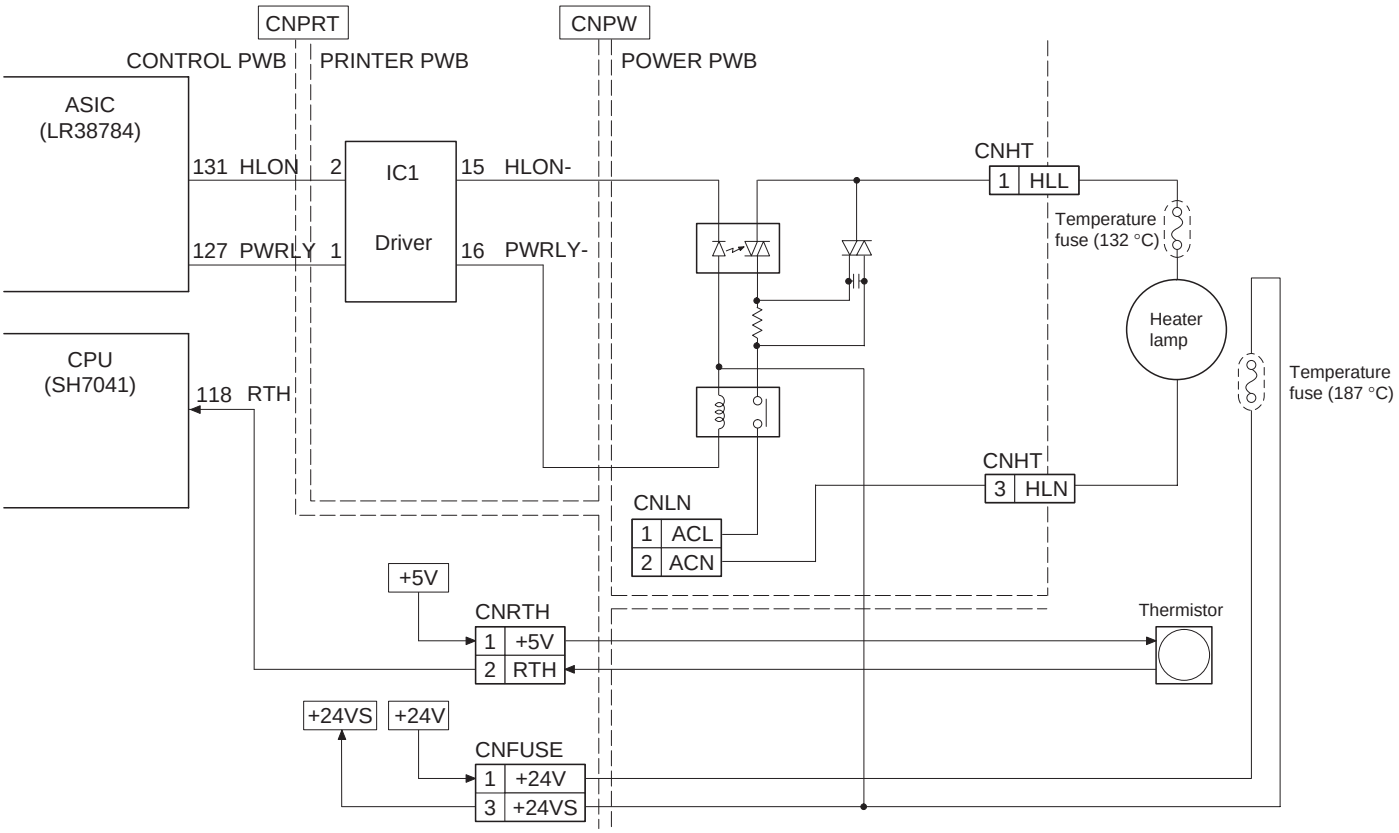


Fig. 16

- The heat roller surface temperature is maintained to the optimum level by controlling ON/OFF of the heater lamp according to the temperature data (voltage) from the thermistor. The heat roller surface temperature is controlled to 155°C. Two temperature fuses are provided to protect the heat machine from an abnormally high temperature in the fusing section. The heater lamp is lighted by the AC power.

j. Timing chart

• Printing process

Pre-revolution processing

Timing from DPAGE (internal signal of ASIC) to BIAS ON (pre-revolution processing) is specified.

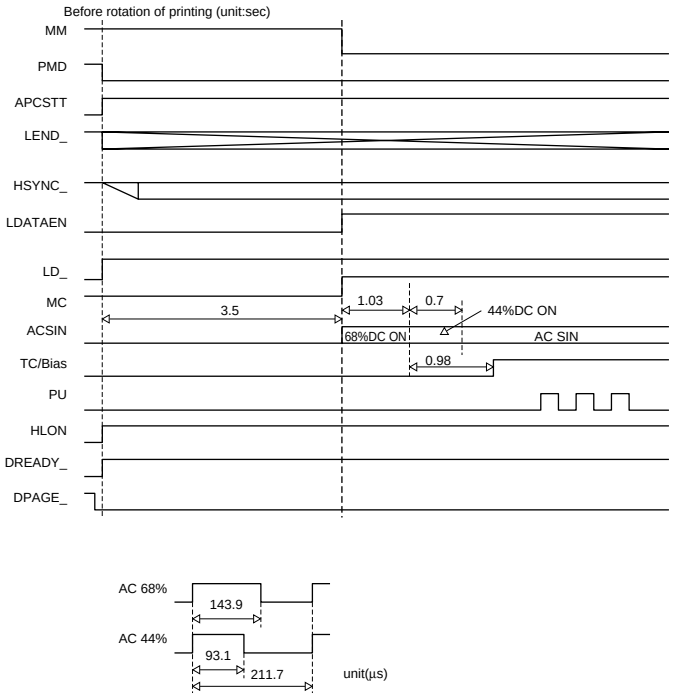


Fig. 17

Laser control becomes hard control from the movement when HSYNC interruption was permitted.

Post-revolution processing

Timings from POUT to motor stop (post-revolution processing for printing) are specified.

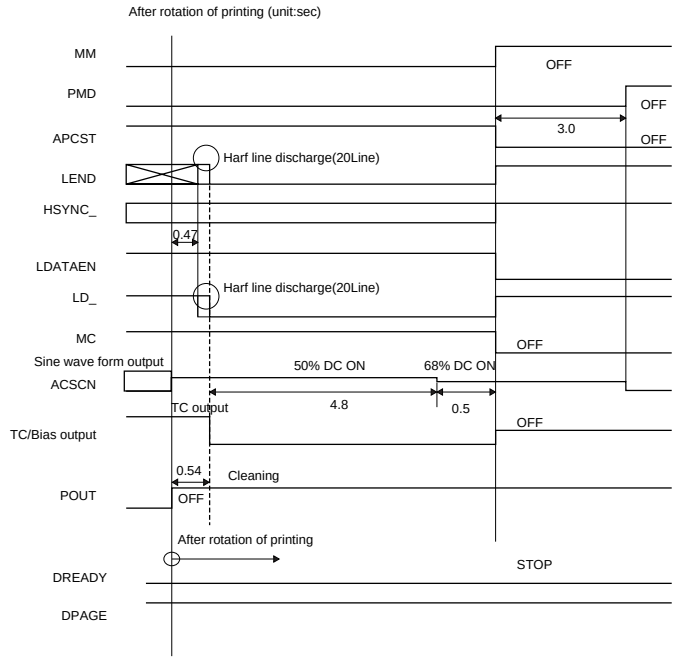


Fig. 18

Continuous printing processing

*1 Waiting according to fixing temperature (Environmental temperature)

*2 Top margin

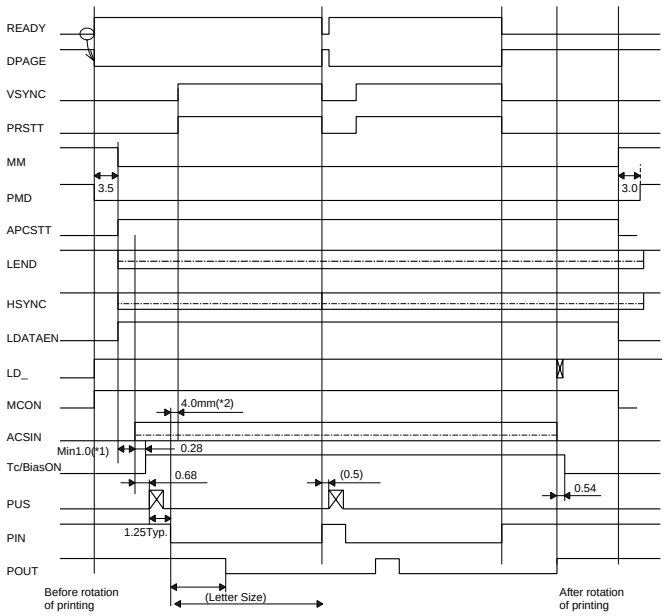


Fig. 19

Revolution before cleaning when power is on and cover is closed

Unit: second

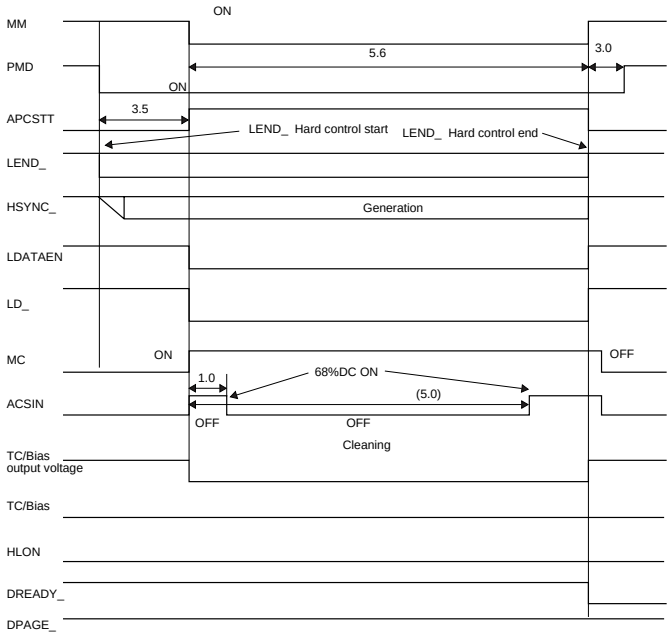


Fig. 20

k. Top margin control

Top margin is set according to the number of lines (the number of HSYNC interrupt) from detail paper Pin On to LASER input.

The interval between Pin On and point D is 52.6747 mm.

The interval between Point D and point B is: 27.33 (C-D) + 8.3769 (B-C) = 35.7069 mm

If top margin is 4 mm,

52.6747 - 35.7069 + 4 = 20.9678 m

In case of the actual software processing, chattering of the sensor is considered to be observed for 9 msec.

The processing speed is 50 mm/sec; while chattering is being observed, paper is fed by 0.45 mm (9 x 50/1000 = 0.45 mm).

In order to gain top margin of 4 mm, printing data should be processed after paper is fed by 20.5178 mm (20.9678 – 0.45 = 20.5178 mm) following PIN On detection.

The base machine resolution in the sub-scanning direction is 391.16 dpi; If the value 20.5178 mm is converted into the number of lines, 315.9 lines are obtained from 391.16 x 20.5178/25.4. Accordingly the software set value is considered to be based on 316 lines.

Similarly, considering from the fact that resolution of PC printing is 600 dpi, the number of lines is 484.6 lines (600 x 20.5178/25.4=484.6). The software set value is based on 485 lines.

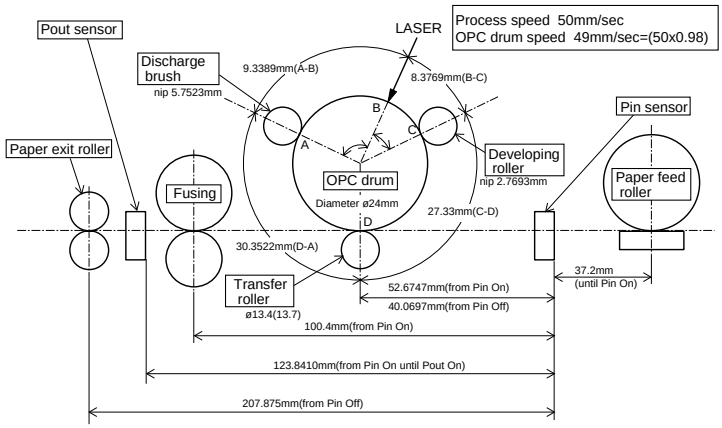


Fig. 21

l. Modem (FM214) block

INTRODUCTION

The conexant FM214 MONOFAX modem is a synchronous 14400 bits per second (bps) half-duplex ,modem with error detection and DTMF reception. It has low power consumption and requires +5V, +3.3V DC power supply. The modem is housed in a signal VLSI device package.
The modem can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).
The FM214 is designed for use in Group 3 facsimile machines.
The modem satisfies the requirements specified in CCITT recommendations V.29, V.27 ter, V.21 Channel 2 and T.4, and meets the binary signaling requirements of T.30.
The modem can operate at 14400, 9600, 7200, 4800, 2400, or 300bps, and also includes V.27 ter short training sequence option.
The modem can also perform HDLC framing according to T.30 at 14400, 9600, 7200, 4800, 2400, or 300 bps.
The modem features a protectors which operate concurrently with the V.21 channel 2 receiver.
The voice mode allows the host computer to efficiently transmit and receive audio signals and messages.
General purpose input/output (GPIO) pins are available for host assignment in the 128 pin PQFP.
The modem's small size, single voltage supply, and low power consumption allow the design of compact system enclosures for use in both office and home environments.
MONOFAX is a registered trademark of conexant systems, Inc.

FEATURES

• Group 3 facsimile transmitting/receiving
- ITU-TV. 17, V. 33 (Model FM214)
- ITU-TV. 29, V. 27 ter, T.30, V. 21 channel 2, T.4
- ITU-TV. 17 and V. 27 ter short train
- HDLC framing at every speed
- Receiving dynamic range: 0 dBm to -43 dBm
- Automatic adaptation equalizer
- Fixed/programmable digital equalizer
- DMTF detection and tone detection
- ITU-TV, 21 channel 2 FSK 7E flag detection
- Ring detector
- Programmable transmission level
- Programmable single/dual tone transmission
• Room monitor
- DTMF detection, tone detection and tone transmission
- Type II transmitter ID CAS detection
- Near-end echo cancellation
- Monitor recording /message reproducing by voice or audio codec
• V.23 and Type I transmitter ID
- Duplex mode
TX = 75 bps, RX = 1200 bps
TX = 1200 bps, RX = 75 bps
• Half duplex mode
TX = RX = 1200 bps
- Serial/parallel data mode
- Programmable parallel data mode
- Data bit 5, 6, 7, or 8
- Stop bit 1 or 2
- Mark, space, even number and odd number parity
- Break function
- Transmitter sequence routine
- Fixed equalizer
• Programmable interface memory
• General input pin (GPI) 8 and general output pin (GPO) 8
• DTE interface: 2 ports
- Selective microprocessor bus (6500 or 8085)
- ITU-T V. 24 (EIA/TIA-232-E interchangeability) interface
• TTL and CMOS interchangeability
• 3.3V/5V performance
• Consumption power
- Operating mode: 200 mW (standard), 275 mW (-V option), 300 mW (-S option)
- Sleep mode: 1 mW (-V option, -VS option)
• Package
- 128 pin TQFP

FM214 (IC8) Terminal description

PIN	I/O	Signal	Function
1	MI	SR41N/RESERVED	Modem Interconnect
2	MI	SR3OUT/RESERVED	Modem Interconnect
3	OA	EYESYNC	Eye Pattern Circuit
4	OA	EYECLK	Eye Pattern Circuit
5	OA	RXD	DTE serial interface
6	MI	SR1IO	Modem Interconnect
7	–	NC	No Connection
8	OA	EYEXY	Eye Pattern Circuit
9	MI	SR4OUT	Modem Interconnect
10	PWR	VDD1	3.3V DIGITAL SUPPLY for DSP.
11	OB	PLSD#	DTE Serial Interface
12	OB	DCLK	DTE Serial Interface
13	IA	EN85#	Host Parallel Interface
14	IA	GPI0	Host Parallel Interface
15	IA	RTS#	DTE Serial Interface
16	GND	DGND1	DSP Digital Ground
17	IA	TXD	DTE Serial Interface
18	MI	SA1CLK	Modem Interconnect
19	IB	RS4	Host Parallel Interface
20	IB	RS3	Host Parallel Interface
21	IB	RS2	Host Parallel Interface
22	IB	RS1	Host Parallel Interface
23	IB	RS0	Host Parallel Interface
24	I	YCLK	
25	MI	IACLK	Modem Interconnect
26	MI	IA1CLK	Modem Interconnect
27	MI	CTRLSIN_S/NC	Modem Interconnect
28	MI	RESERVED/NC	Modem Interconnect
29	MI	SOUT_S/NC	Modem Interconnect
30	MI	SIN_S/NC	Modem Interconnect
31	MI	FSYNC_S/NC	Modem Interconnect
32	MI	IARESET_S#/NC	Modem Interconnect
33	GND	AGND1	IA Analog Ground
34	I	LINEIN_S/NC	Line Interface
35	I	MICP_S/NC	Microphone Input
36	I	MICM_S/NC	Microphone Input
37	O	MICBIAS_S/NC	Microphone Bias Output
38	–	NC	No Connection
39	–	NC	No Connection
40	MI	VREF_S/NC	Modem Interconnect
41	MI	VC_S/NC	Modem Interconnect
42	PWR	VAA_S/NC	5V IA Analog power
43	O	LINEOUT_S/NC	Line Interface
44	–	NC	No Connection
45	GND	AGND2	IA Analog Ground
46	O	SPKRP_S/NC	Speaker Interface Output
47	O	SPKRM_S/NC	Speaker Interface Output
48	PWR	AVDD_S/NC	3.3V IA Digital power
49	MI	RESERVED/NC	Modem Interconnect
50	MI	ICLK_S/NC	Modem Interconnect
51	MI	MCLK_P	Modem Interconnect
52	MI	CTRLSIN_P	Modem Interconnect
53	MI	RESERVED	Modem Interconnect
54	MI	SOUT_P	Modem Interconnect
55	MI	SIN_P	Modem Interconnect
56	MI	FSYNC_P	Modem Interconnect
57	MI	IARESET_P#	Modem Interconnect
58	GND	AGND3	IA Analog Ground
59	–	NC	No Connection
60	I	LINEIN_P	Line Interface
61	I	MICP_P	Microphone Input
62	I	MICM_P	Microphone Input
63	O	MICBIAS_P	Microphone Bias Output
64	–	NC	No Connection
65	NC	NC	No Connection
66	MI	VREF_P	Modem Interconnect
67	MI	VC_P	Modem Interconnect
68	PWR	VAA_P	5V Analog Supply for IA
69	O	LINEOUT_P	Line Interface
70	GND	AGND4	IA Analog Ground
71	O	SPKRP_P	Speaker Interface Output
72	O	SPKRM_P	Speaker Interface Output
73	PWR	AVDD_P	3.3V Digital power for IA
74	–	NC	No Connection
75	MI	ICLK_P	Modem Interface
76	MI	MCLK_S/NC	Modem Interface
77	PWR	VDD2	3.3V Digital Supply for DSP
78	IB/OC	D7	Host Parallel Interface
79	IB/CC	D6	Host Parallel Interface
80	IB/OC	D5	Host Parallel Interface
81	IB/OC	D4	Host Parallel Interface
82	IB/OC	D3	Host Parallel Interface
83	IB/OC	D2	Host Parallel Interface
84	GND	DGND2	DSP Digital Ground
85	PWR	VDD3	3.3V Digital Supply for DSP
86	IB/OC	D1	Host Parallel Interface
87	GND	DGND3	DSP Digital Ground
88	IB/OC	D0	Host Parallel Interface
89	IB	CSBR#	Host Parallel Interface
90	IB	WRITE#	Host Parallel Interface
91	IB	CS#	Host Parallel Interface
92	IB	READ#	Host Parallel Interface
93	IA	GPI2	General purpose input
94	IA	GP13	General purpose input
95	IA	GP14	General purpose input
96	IA	GP15	General purpose input
97	IA	GP16	General purpose input
98	IA	GP17	General purpose input
99	OC	GPO7	General purpose input
100	PWR	VDD4	3.3V DSP Digital Power
101	OC	GPO6	General purpose output
102	OC	GPO5	General purpose output
103	MI	RESERED	Modem Interconnect
104	OC	GPO4	General purpose output
105	OC	GPO3	General purpose output
106	GND	DGND4	DSP Digital Ground
107	OB	CTS#	DTE Serial Interface

FM214 (IC8) Terminal description

PIN	I/O	Signal	Function
108	OB	IRQ1#	Interrupt request
109	OC	GPO2	General purpose output
110	OC	GPO1	General purpose output
111	OC	GPO0	GPO0 (IA reset)
112	PWR	VDD5	3.3V DSP Digital Power
113	PWR	VGG	5V DSP Digital
114	GND	DGND5	DSP Digital Ground
115	IB	RESET#	External reset
116	I	XTALI	Crystal in
117	O	XTALO	Crystal out
118	MI	RESERVED	Modem Interconnect
119	OB	XCLK	X clock output
120	IA	GPI1	General purpose input
121	OA	IRQ2#	Interrupt request
122	MI	SR3IN	Modem Interconnect
123	MI	RESERVED	Modem Interconnect
124	MI	RESERVED	Modem Interconnect
125	GND	DGND6	DSP Digital Ground
126	PWR	DVAA	3.3V DSP analog power
127	GND	AGND5	DSP Analog Ground
128	MI	RESERVED	Modem Interconnect

Note:
I/O:
MI = Modem interconnect
IA, IB = Digital input
OA, OB, OC = Digital output
I = Analog input
O = Analog output
–P signal: Primary IA
_S signal: Secondary IA
Reserved = Not connect

m. Image signal process block

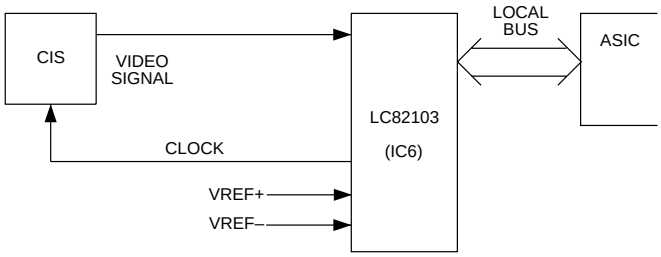


Fig. 22

The CIS is driven by the LSI (LC82103), and the output video signal from the CIS in input into the LC82103.
The ADC and buffer are provided in the LC82103, and the digital image processing is performed.

n. Speaker amplifier

The speaker amplifier monitors the line under the on-hook mode, outputs the buzzer sound generated from the SH7041, ringer sound, DTMF generated from the modem, and line sound.

o. Adjustment of voice/ringer volume

The voice/ringer volume can be adjusted by using the panel buttons “UP” and “DOWN”.

- The ringer volume can be adjusted in the Stand-by mode by pressing the UP/DOWN button.
- The reception level can be adjusted by pressing the UP/DOWN button when the handset is located in the off-hook state.
- The speaker volume can be adjusted by using the speaker key.

[3] Circuit description of TEL/LIU and Hook SW PWB

1. TEL/LIU block operation description

(1) Block diagram

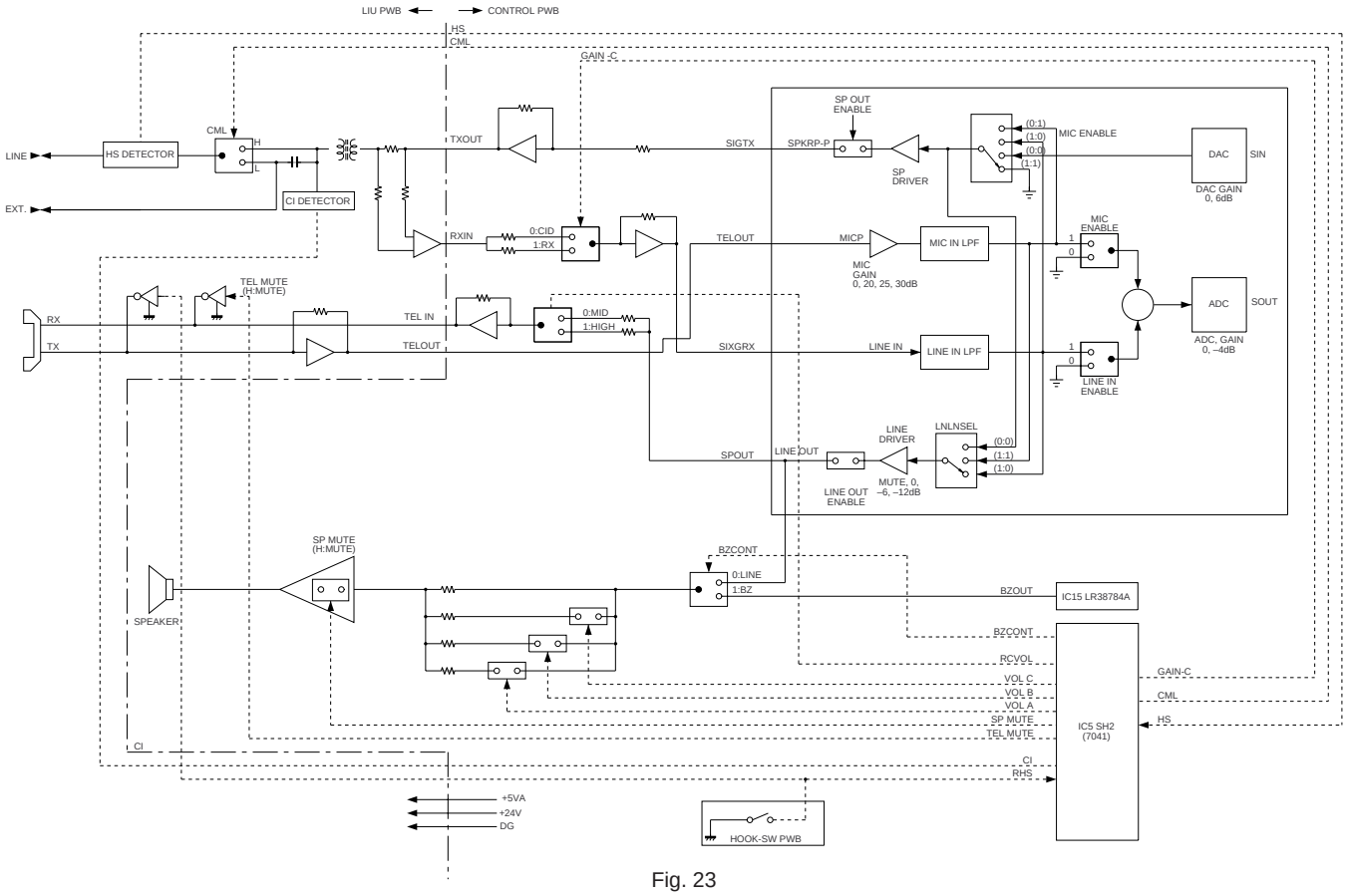


Fig. 23

(2) Circuit description

The TEL/LIU PWB is composed of the following 9 blocks.
1. Surge protection circuit
2. On-hook status detection circuit
3. Dial pulse generation circuit
4. CML relay
5. Matching transformer
6. Hybrid circuit
7. Signal selection
8. CI detection circuit
9. Power supply and bias circuit

(3) Block description

1) Surge Protection circuit

This circuit protects the circuit from the surge voltage occurring on the telephone line.

- The AR1 protects the circuit from the 390V or higher line surge voltages.
- The VA1 and VA2 protect the circuit from the 470V or higher vertical surge voltage.

2) On-hook status detection circuit

The on-hook status detection circuit detects the status of the hook switch (RHS) of built-in telephone, and the status of the hook of a telephone externally connected.

- The status of on-hook switch ($\overline{RHS}$) is determined from the logical level of $\overline{RHS}$ signal. ($\overline{RHS}$ is in the hook SW PWB)

$\overline{RHS}$ LOW: ON-HOOK

$\overline{RHS}$ HIGH: OFF-HOOK

- External telephone hook status detection circuit ($\overline{HS}$)

This circuit comprises the photo-coupler PC2, resistors R1 and R2, Zener diodes ZD1 and ZD2.

When an external telephone is connected and enters the on-hook mode, the LED of photo-coupler PC2 emits light and the light receiving element turns on. The status signal $\overline{HS}$ is input to the pin119 of (SH7041) (IC5: control PWB).

$\overline{HS}$ LOW: EXT. TEL OFF-HOOK

$\overline{HS}$ HIGH:EXT. TEL ON-HOOK

3) Dial pulse generation circuit

The pulse dial generation circuit comprises the CML relay.

4) CML relay

The CML relay switches over connection to the matching transformer T1 while the FAX or built-in telephone is being used.

5) Matching transformer

The matching transformer performs electrical insulation from the telephone line and impedance matching for transmitting the TEL/FAX signal.

6) Hybrid circuit

The hybrid circuit performs 2-wire-to-4-wire conversion using the IC1 of operational amplifier, transmits the voice transmission signal to the line, and feeds back the voice signal to the voice reception circuit as the side tone.

7) Signal selection

The following signals are used to control the transmission line of TEL/FAX signal. For details, refer to the signal selector matrix table.

[Control signals from output port]

<table>
<tr><th>Signal Name</th><th>Description</th></tr>
<tr><td>CML</td><td>Line connecting relay and DP generating relay
H: Line make
L: Line break</td></tr>
<tr><td>SP MUTE</td><td>Speaker tone mute control signal
H: Muting (Power down mode)
L: Muting cancel (Normal operation)</td></tr>
<tr><td>TEL MUTE</td><td>Handset reception mute control signal
H: Muting
L: Muting cancel</td></tr>
<tr><td>RCVOL
(The circuit is located in the control PWB.)</td><td>Handset receiver volume control signal
<table>
<tr><th>Volume</th><th>High</th><th>Middle</th><th>Low</th></tr>
<tr><td>RCVOL</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td></td><td></td><td></td><td>*</td></tr>
</table>
* Set the line driver of MODEM (FM214) to – 6 dBm</td></tr>
<tr><td>VOL A
VOL B
VOL C
(The circuit is located in the control PWB.)</td><td>Speaker volume control signal
VRSEL1 VRSEL2 matrix
<table>
<tr><th></th><th>VOL A</th><th>VOL B</th><th>VOL C</th><th>RING./ Receiving</th><th>Buzzer</th><th>DTMF</th></tr>
<tr><td></td><td>H</td><td>L</td><td>L</td><td>High</td><td>—</td><td>High</td></tr>
<tr><td></td><td>L</td><td>H</td><td>L</td><td>Middle</td><td>—</td><td>Middle</td></tr>
<tr><td></td><td>L</td><td>L</td><td>H</td><td>Low</td><td>—</td><td>Low</td></tr>
<tr><td></td><td>L</td><td>L</td><td>L</td><td>—</td><td>Fixed</td><td>—</td></tr>
</table></td></tr>
<tr><td>GAIN-C
(The circuit is located in the control PWB.)</td><td>Reception gain switching signal
L: When connected to line, 1: 1 gain
H: When not connected to line, HIGH gain</td></tr>
<tr><td>BZCONT
(The circuit is located in the control PWB.)</td><td>Speaker output signal switching
H: Buzzer signal output
L: When monitoring line signal</td></tr>
</table>

[Signals for status recognition according to input signals]

Signal Name	Function
$\overline{\text{RHS}}$ (On the HOOK-SW PWB)	H: The handset is in the on-hook state. L: The handset is in the off-hook state.
CI	Incoming call (CI) detection signal.
$\overline{\text{HS}}$	H: The handset or external telephone is in the on-hook state. L: The handset or external telephone is in the off-hook state.

[Other signals]

Signal Name	Function
TEL IN	Receiving signal from line or modem
TEL OUT	Transfer signal to line
TXOUT	Transmission (DTMF) analog signal output from modem
RXIN	Reception (DTMF, others) analog signal input into modem

No.	Signal Name (CNLIU)	No.	Signal Name (CNLIU)
1	+24V	7	$\overline{\text{RHS}}$
2	DG	8	TXOUT
3	+5VA	9	RXIN
4	CML	10	TELMUTE
5	$\overline{\text{CI}}$	11	TELOUT
6	$\overline{\text{HS}}$	12	TELIN

No.	Signal Name (CNHS 1 and 2)	No.	Signal Name (CNHS 1 and 2)
1	$\overline{\text{RHS}}$	2	DG

8) CI detection circuit

The CI detection circuit detects the CI signals of 15.3 Hz to 68 Hz. A CI signal, which is provided to the photo-coupler PC1 through the C3 (0.82 uF), R5 (22 K), and ZD3 when the ring signal is inputted from the telephone line.

9) Power supply and bias circuits

The voltages of +5VA and +24V are supplied from the control PWB unit.

(Example: Fax signal send)

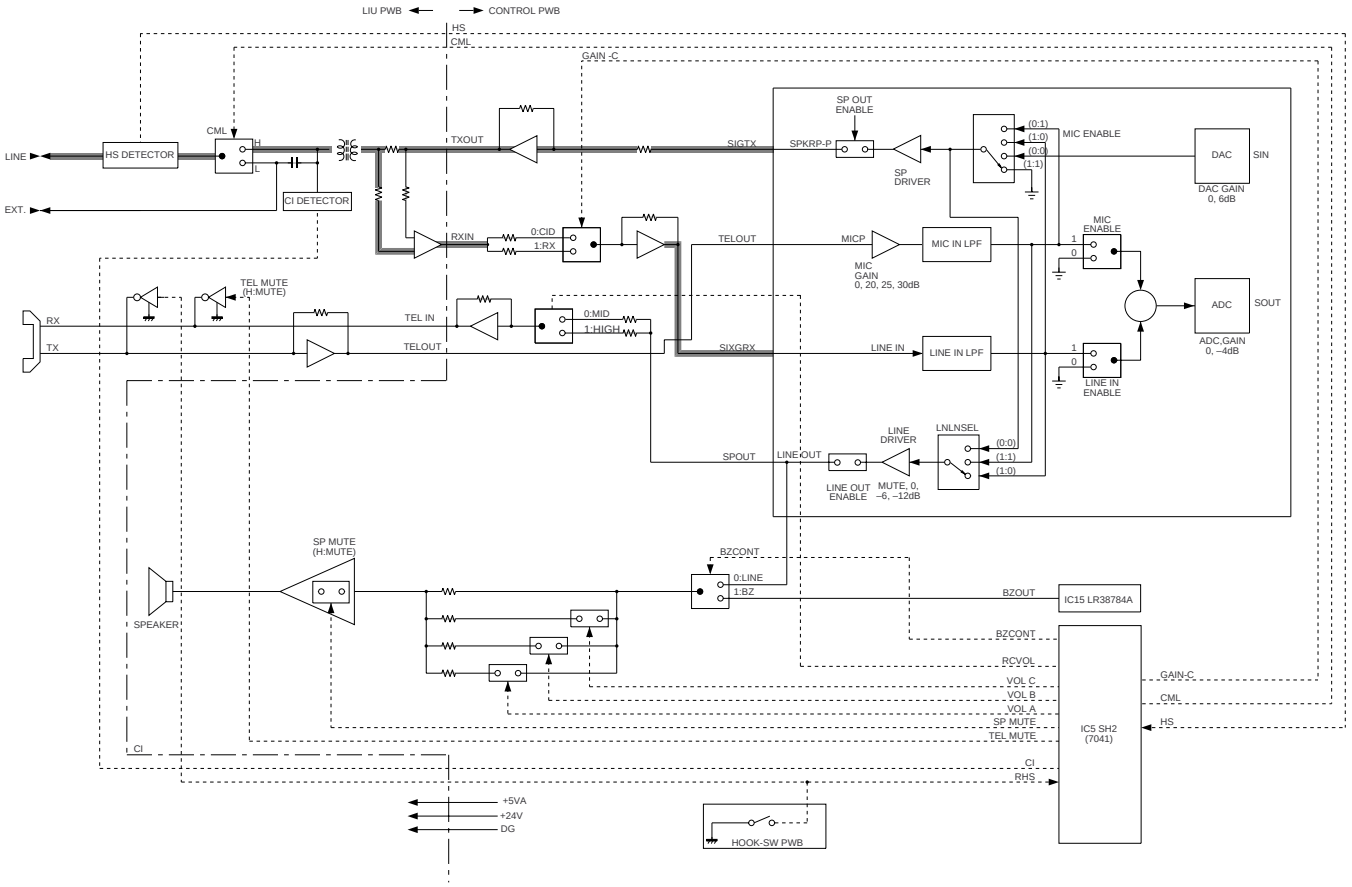


Fig. 24

[4] Circuit description of power supply PWB

1. Noise filter circuit

The filter part removes noises generated from the power unit to avoid noise release outside and prevent external noises from entering. Excessive surge such as thunder is prevented by varistor Z1.

2. Rectified smoothing circuit

The rectified smoothing circuit rectifies AC input at diodes D10, 11, 12, and 13, and then smoothens it at capacitor C5 to supply DC voltage to the switching part.

3. Switching part

This circuit adopts the ringing choke converter system of self-excited type.

By repeating ON/OFF of MOS FETQ1, this system converts DC voltage supplied from the rectified smoothing part into high-frequency pulse, stores energy in the primary winding of transformer T1 during ON period, releases energy to the secondary winding during OFF period, and supplies power.

Frequency changes according to output load; As load increases, ON period becomes longer.

Constant voltage is controlled by applying feedback to the control circuit via photo coupler from 24 V output.

The overcurrent protective circuit detects prolonged ON period caused by excessive output load, lengthens Q1 OFF period by using the control circuit, and restricts energy stored in the primary winding of transformer T1.

Increase of the secondary output voltage 24 V is led to the overcurrent condition by turning on power zener diode D202 between 24 V output and GND.

Thus overvoltage is protected by operating the overcurrent protective circuit of the control circuit.

4. 24 V circuit

To supply output, transformer T1 output is rectified and smoothened with the use of diode D101 and capacitor C101. Voltage is controlled by Volume VR101.

5. +5 V circuit

Transformer T1 output is rectified and smoothened with the use of diode D301 and capacitor C301 to stabilize +5 V output by using 3-terminal regulator IC301.

6. Heater circuit

To maintain the optimal temperature, the heater lamp is controlled by HLON signal from the control panel.

This HLON signal is to switch ON/OFF the heater lamp. If this signal is input LOW, PC2 is switched ON, resulting TRIACK TRA1 ON.

Accordingly, AC power is supplied to the heater lamp to switch the heater lamp ON.

7. Zero cross circuit

When AC input reaches the zero cross point (0 V), PC3 is switched ON. When Q501 is switched ON, the zero cross signal is output to the control panel.

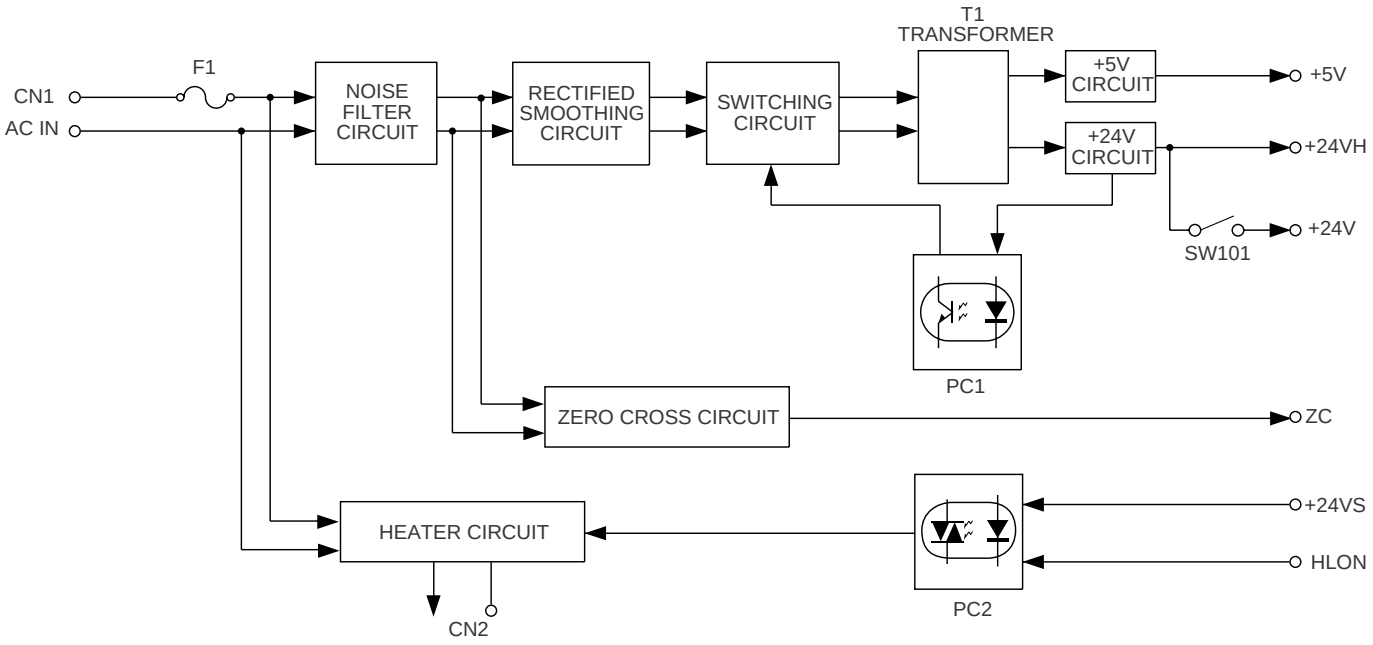


Fig. 25

[5] Circuit description of CIS UNIT

This CIS unit picks up optical information from the document, converts it into an electrical (analog) signal and it to the control PWB.

1. Block diagram

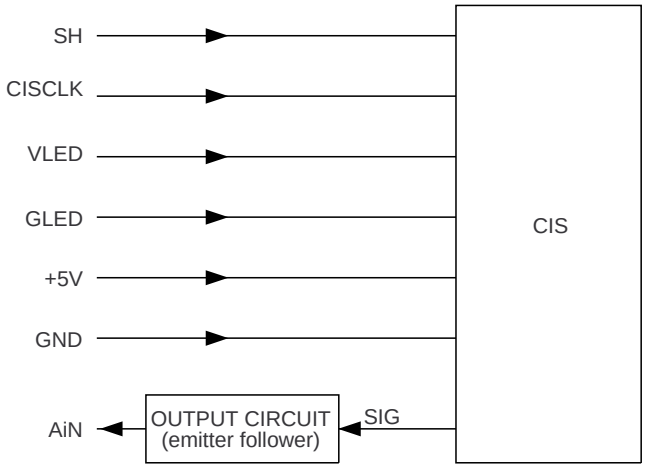


Fig. 26

2. Description of blocks

(1) CIS

The DL100-05AUJC is highly sensitive charged coupled image sensor that consists of 1728 picture elements.

Receiving two drive signal (SI,CLK) from the control PWB, the transferred photoelectric analog signal SIG is impedance converted, and the signal AIN, is supplied to the control PWB.

(2) Waveforms

1. CLK, SI, SIG signals within the control PWB.

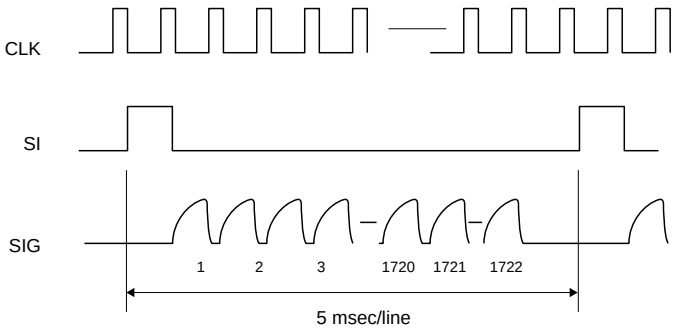


Fig. 27